

SNES S-DSP Pinout by [Jonathon W. Donaldson \(jwdonal\)](#) (special thanks to [Martin Korth \(nocash\)](#))

Designator	Name	Desc	QFP80P1870X2470-80M	Type	Owner	Show	Number	Name
1	DKD	(5 clks = 1.2us) 4.096MHz (24.576MHz/6) (NC)	1	Output	1	True	True	DKD
2	MXK	(5 clks = 1.6us) 3.072MHz (24.576MHz/8) (NC)	2	Output	1	True	True	MXK
3	MX1	24.576MHz/24 (3pins: phase/duty shifted) (NC)	3	Output	1	True	True	MX1
4	MX2	24.576MHz/24 (3pins: phase/duty shifted) (NC)	4	Output	1	True	True	MX2
5	MX3	24.576MHz/24 (3pins: phase/duty shifted) (NC)	5	Output	1	True	True	MX3
6	MD2	SMP/DSP Multiplexed SRAM Data	6	I/O	1	True	True	MD2
7	MD1	SMP/DSP Multiplexed SRAM Data	7	I/O	1	True	True	MD1
8	MD0	SMP/DSP Multiplexed SRAM Data	8	I/O	1	True	True	MD0
9	MA0	SMP/DSP Multiplexed SRAM Address	9	Output	1	True	True	MA0
10	MA1	SMP/DSP Multiplexed SRAM Address	10	Output	1	True	True	MA1
11	MA2	SMP/DSP Multiplexed SRAM Address	11	Output	1	True	True	MA2
12	VSS	Supply	12	Power	1	True	True	VSS
13	MA3	SMP/DSP Multiplexed SRAM Address	13	Output	1	True	True	MA3
14	MA4	SMP/DSP Multiplexed SRAM Address	14	Output	1	True	True	MA4
15	MA5	SMP/DSP Multiplexed SRAM Address	15	Output	1	True	True	MA5
16	MA6	SMP/DSP Multiplexed SRAM Address	16	Output	1	True	True	MA6
17	MA7	SMP/DSP Multiplexed SRAM Address	17	Output	1	True	True	MA7
18	MA12	SMP/DSP Multiplexed SRAM Address	18	Output	1	True	True	MA12
19	MA14	SMP/DSP Multiplexed SRAM Address	19	Output	1	True	True	MA14
20	MA15	SMP/DSP Multiplexed SRAM Address (NC) (instead, upper/lower 32KB selected via /CE1 and /CE0)	20	Output	1	True	True	MA15
21	DIP	Unknown (always high?) (NC)	21	Passive	1	True	True	DIP
22	MD3	SMP/DSP Multiplexed SRAM Data	22	I/O	1	True	True	MD3
23	MD4	SMP/DSP Multiplexed SRAM Data	23	I/O	1	True	True	MD4
24	MD5	SMP/DSP Multiplexed SRAM Data	24	I/O	1	True	True	MD5
25	MD6	SMP/DSP Multiplexed SRAM Data	25	I/O	1	True	True	MD6
26	MD7	SMP/DSP Multiplexed SRAM Data	26	I/O	1	True	True	MD7
27	C\E1\	SMP/DSP Multiplexed	27	Output	1	True	True	C\E1\

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28	C\E\0	SRAM Chip-Enable (Active-Low) (to upper 32KB) SMP/DSP Multiplexed SRAM Chip-Enable (Active-Low) (to lower 32KB)	28	Output	1	True	True	C\E\0
29	MA10	SMP/DSP Multiplexed SRAM Address	29	Output	1	True	True	MA10
30	O\E\	SMP/DSP Multiplexed SRAM Output-Enable (Active-Low)	30	Output	1	True	True	O\E\
31	MA11	SMP/DSP Multiplexed SRAM Address	31	Output	1	True	True	MA11
32	MA9	SMP/DSP Multiplexed SRAM Address	32	Output	1	True	True	MA9
33	VCC	Supply	33	Power	1	True	True	VCC
34	MA8	SMP/DSP Multiplexed SRAM Address	34	Output	1	True	True	MA8
35	MA13	SMP/DSP Multiplexed SRAM Address	35	Output	1	True	True	MA13
36	W\E\	SMP/DSP Multiplexed SRAM Write-Enable (Active-Low)	36	Output	1	True	True	W\E\
37	TF	Unknown (GND) (wiring TF and/or TK to VCC crashes the SPC700, ie. they seem to mess up CPUK clock or SRAM bus)	37	Input	1	True	True	TF
38	TK	Unknown (GND) (wiring TF and/or TK to VCC crashes the SPC700, ie. they seem to mess up CPUK clock or SRAM bus)	38	Input	1	True	True	TK
39	MU\T\E\	Mute (to audio amplifier circuit)	39	Output	1	True	True	MU\T\E\
40	MCK	64000Hz (24.576MHz/24/16) (NC)	40	Output	1	True	True	MCK
41	SCLK	3.072MHz (24.576MHz/8) (via inverters to CIC chip)	41	Output	1	True	True	SCLK
42	BCK	DAC Bit Clock, 1.536MHz (24.576/16) (to uPD6376)	42	Output	1	True	True	BCK
43	LRCK	DAC Left/Right Clock, 32000Hz (24.576MHz/16/48) (to uPD6376)	43	Output	1	True	True	LRCK
44	DATA	DAC Serial Data (8xZeroPadding+16xData) (to uPD6376)	44	Output	1	True	True	DATA
45	XTALO	24.576MHz Osc	45	Output	1	True	True	XTALO
46	XTALI	24.576MHz Osc	46	Input	1	True	True	XTALI
47	R\E\S\E\T	Reset (Active-Low) (from System)	47	Output	1	True	True	R\E\S\E\T
48	CPUK	2.048MHz (24.576MHz/12) (to S-SMP)	48	Output	1	True	True	CPUK
49	PD2	Unknown (likely SRAM Data tri-state control signal or CPU/DSP enable)	49	Passive	1	True	True	PD2

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50	PD3	(to/from S-SMP) Unknown (likely SRAM Data tri-state control signal or CPU/DSP enable) (to/from S-SMP)	50	Passive	1	True	True	PD3
51	D0	S-SMP SRAM Data	51	I/O	1	True	True	D0
52	VSS	Supply	52	Power	1	True	True	VSS
53	D1	S-SMP SRAM Data	53	I/O	1	True	True	D1
54	D2	S-SMP SRAM Data	54	I/O	1	True	True	D2
55	D3	S-SMP SRAM Data	55	I/O	1	True	True	D3
56	D4	S-SMP SRAM Data	56	I/O	1	True	True	D4
57	D5	S-SMP SRAM Data	57	I/O	1	True	True	D5
58	D6	S-SMP SRAM Data	58	I/O	1	True	True	D6
59	D7	S-SMP SRAM Data	59	I/O	1	True	True	D7
60	A0	S-SMP SRAM Address	60	Input	1	True	True	A0
61	A1	S-SMP SRAM Address	61	Input	1	True	True	A1
62	A2	S-SMP SRAM Address	62	Input	1	True	True	A2
63	A3	S-SMP SRAM Address	63	Input	1	True	True	A3
64	A4	S-SMP SRAM Address	64	Input	1	True	True	A4
65	A5	S-SMP SRAM Address	65	Input	1	True	True	A5
66	A6	S-SMP SRAM Address	66	Input	1	True	True	A6
67	A7	S-SMP SRAM Address	67	Input	1	True	True	A7
68	A8	S-SMP SRAM Address	68	Input	1	True	True	A8
69	A9	S-SMP SRAM Address	69	Input	1	True	True	A9
70	A10	S-SMP SRAM Address	70	Input	1	True	True	A10
71	A11	S-SMP SRAM Address	71	Input	1	True	True	A11
72	A12	S-SMP SRAM Address	72	Input	1	True	True	A12
73	VCC	Supply	73	Power	1	True	True	VCC
74	A13	S-SMP SRAM Address	74	Input	1	True	True	A13
75	A14	S-SMP SRAM Address	75	Input	1	True	True	A14
76	A15	S-SMP SRAM Address	76	Input	1	True	True	A15
77	XCK	24.576MHz (24.576MHz/1) (NC)	77	Output	1	True	True	XCK
78	DCK	8.192MHz (24.576MHz/3) (to Expansion Port)	78	Output	1	True	True	DCK
79	CK1	12.288MHz (24.576MHz/2) (NC)	79	Output	1	True	True	CK1
80	CK2	6.144MHz (24.576MHz/4) (NC)	80	Output	1	True	True	CK2